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ABSTRACT

The aim of the regional research project SIMPAA2, which continues the former national research SIMPAA project, is the realization of a hardware simulator of MIMO propagation channels for UMTS and WLAN applications. The simulator must reproduce the behavior of the radio propagation channel, thus making it possible to test "on table" the mobile radio equipments. The advantages are: low cost, short test duration, possibility to ensure the same test conditions in order to compare the performance of various equipments.

I. INTRODUCTION

During last years, the development of wireless technologies offers many prospects and new applications. This trend will be accentuated in the future, the systems still having to improve their data rate and mobility. UMTS (Universal Mobile Telecommunications System) and WLAN (Wireless Local Area Networks) constitute the mobile and wireless telecommunications systems of third generation and beyond able to offer to general public the high-rate multi-media services. MIMO (Multiple-Input Multiple-Output) systems make use of antenna arrays at both the transmit and the receive sides of a radio link to drastically improve the capacity over more traditional systems.

However, the transmitted electromagnetic waves interact with the propagation environment (indoor/outdoor). It is thus necessary to take into account the main propagation parameters during the design of the future communication systems. The optimal choice of the modulation, coding, etc. for these communication systems is based on a reliable model of the radio propagation channel. Moreover, after the realization of a communication system, its experimental performance can be evaluated by using a hardware radio channel simulator. A hardware simulator can also be used to compare the performance of various radio communication systems in a time-variant propagation channel in the same test conditions.

On the market, there are some hardware channel simulators (Propsim, Smart System, Spirent), but they are very expensive and therefore prohibitive for a communication laboratory.

This paper presents the design of the digital block of a hardware simulator for indoor/outdoor MIMO radio channels. Section 2 of the paper deals with the architecture of the digital block of the hardware simulator. This section is divided into three parts: RF blocks, Channel model block and Digital block describing their respective architecture and several parameters useful to design the hardware simulator. Lastly, Section 3 shows the beginning of the realization of the hardware digital block. The prototyping platform is described and simulations carried out give first results. The trade-off between results accuracy, complexity and cost represents an important choice during the design of the digital block of the hardware simulator.

II. HARDWARE SIMULATOR: PRINCIPLE, ARCHITECTURE AND OPERATION

The simulator must reproduce the behavior of a MIMO propagation channel for a specific environment, indoor or outdoor. This makes it possible to check the correct operation of the new radio communication systems and to compare their performances under the same test conditions.

The simulator must operate with RF signals (2 GHz for UMTS and 5 GHz for WLAN). In order to make adjacent channels interference tests for UMTS systems, it is useful to consider three successive channels, thus to have a 3x5 MHz bandwidth. Therefore, the frequency bandwidths B are 15 MHz for UMTS and 20 MHz for WLAN.

Moreover, UMTS uses two operating modes: the TDD mode (Time Division Duplex) having the same frequency band for both uplink and downlink and the FDD mode (Frequency Division Duplex) having different frequency bands. In addition, depending on the strength of the transmitted signals, the simulator must be able to accept input signals with wide power range, between - 50 and 33 dBm, which implies a power control for the simulator inputs.

The design and realization of the RF block for UMTS systems were completed in the previous SIMPAA (SImulateur Matériel de Propagation pour Antennes Adaptatives) project [1]. The RF block will need some modifications required by WLAN specifications. The objectives of the actual regional project SIMPAA2 mainly concern the channel model block and the digital block of the MIMO simulator, as shown in Fig. 1 by the gray blocks.

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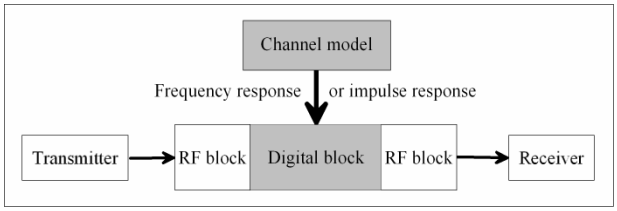

Fig. 1. Block diagram of a one-way SISO channel.

A. RF Blocks

The number of radio frequency blocks is determined by the number of the transmitting and receiving antennas. For a transmitter with N_T antennas and a receiver using N_R antennas, the MIMO simulator must have $N_T N_R$ full-duplex SISO channels, thus 2 $N_T N_R$ one-way SISO channels. The actual choice of 18 one-way SISO channels seems to be a suitable trade-off between utility, complexity and cost, assuming $2 \leq N_T$, $2 \leq N_R$ and $N_T + N_R \leq 6$.

As shown in Fig. 2, for RF receiver and transmitter, the "Attenuator" and "Amplifier" blocks are controlled respectively via "Control bus" and "Gain control bus" in order to adjust the reception and transmission power by the automatic gain control (AGC).

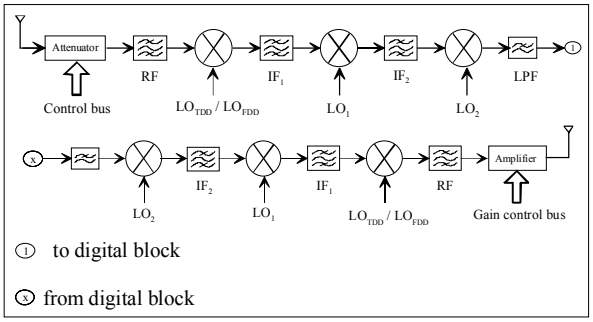

Fig. 2. Reception and transmission RF units for a one-way SISO channel.

In the reception RF unit, local oscillators LO_{TDD} or LO_{FDD} allow the RF to IF_1 conversion by taking into account the TDD and FDD modes which use different frequency bandwidths. Then, the third local oscillator LO_1 allows the IF_1 to IF_2 conversion. The IF_2 band-pass filter must perform a good rejection of the out-of-band frequencies to avoid aliasing problems. The local oscillator LO_2 and the low-pass filter (LPF) give a low-frequency real signal (its Fourier transform keeps the hermitian symmetry). After the digital block, the transmission RF unit converts, with the equivalent steps, the low-pass version of the $y_j(t,\tau)$ signal into a RF signal.

Moreover, when the impulse response or frequency response of the propagation channel presents fadings, their samples must be "amplified" before A/D conversion, in order to obtain a convenient utilisation of the full-scale. This allows a reduction of the computing errors of the digital blocks.

Thus, the final RF amplifier restores the correct level of the signal $y_j(t,\tau)$ received by the j^{th} Rx antenna by taking into account the attenuation introduced by AGC block and the amplification of the impulse or frequency response of the channel.

Fig.3 shows the realization of the RF reception (high part) and transmission (low part) units, as well as the connection unit (left part) which allows the link between antenna and the RF reception and transmission units. This RF block was realized in printed technology during the previous SIMPAA project.

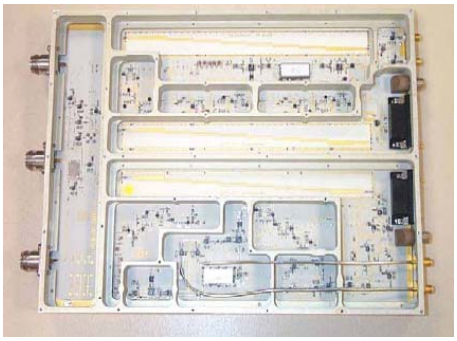

Fig. 3. UMTS receiver and transmitter of a SISO RF block.

B. Channel Model Block

A MIMO channel is composed of several randomly time-variant correlated SISO channels. Fig. 4 illustrates a MIMO channel with $N_T = 2$ transmit antennas and $N_R = 2$ receive antennas.

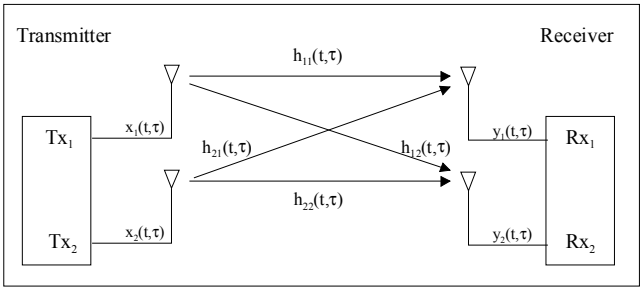

Fig. 4. MIMO channel (2 x 2 SISO channels).

For this MIMO channel, the signal $y_j(t,\tau)$ received by the j^{th} receive antenna can by easily obtained:

$$y_j(t,\tau) = x_1(t,\tau) * h_{1j}(t,\tau) + x_2(t,\tau) * h_{2j}(t,\tau),\ j = 1,2 \quad (1)$$

For a hardware implementation, it is easier to use the Fourier transform to replace the convolution by an algebraic product:

$$Y_j(t,f) = X_1(t,f).H_{1j}(t,f) + X_2(t,f).H_{2j}(t,f),\ j = 1,2 \quad (2)$$

As it was shown in [2], this solution is possible to implement but its disadvantage is the generated latency. For indoor environments, we will consider the first

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relation because a FIR (Finite Impulse Response) filter has, in spite of its relative complexity, a much lower latency. For outdoor environments, the effective duration W_t of the impulse response of the channel is wider. Therefore, in order to reduce the complexity and the cost of the digital block, the second relation is used. Therefore, both approaches can be used according to the considered propagation environment.

The channel models used by the simulator will be obtained from measurements by using a time domain MIMO channel sounder designed and realized at the IETR [3], as shown in Fig. 5.

Fig. 5. MIMO channel sounder.

Fig.6 shows the Uniform Linear Array (ULA) used for outdoor measurements with 4 active elements [4].

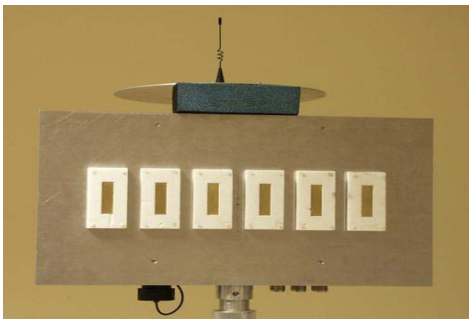

Fig. 6. ULA Tx Antenna.

This MIMO channel sounder is based on the correlation technique [5]. For each SISO channel, the sounder gives the measured complex envelope of its impulse response. During the measurement of all SISO channels, the MIMO channel must be practically invariant. This limits the mobile speed and therefore the maximal value of the Doppler shift.

A simple way to use these measurement results is to compute, for each location of the mobile transmitter, the frequency responses $H_{i,j}(t,f)$ as Fourier transforms of the impulse responses $h_{i,j}(t,\tau)$ of the MIMO propagation channel. These frequency responses can be used to supply the "Channel model" block of each SISO channel, as shown in Fig. 1. Periodically, the frequency responses must be actualized, in order to simulate the channel time-evolution. The "refreshing" period of the frequency responses is determined by the channel coherence time, thus by the mobile speed and the propagation environment. As the number of the recorded files is finite, it will be necessary to periodically replay the whole set of frequency responses.

C. *Digital Block*

For outdoor environments, the impulse responses are longer, thus more points are necessary to describe them. Moreover, the impulse responses are more often refreshed, thus the number of profiles to be stored and treated is more significant. Thus, computations are carried out in the frequency domain because FFT modules need less resources than FIR filters. On the other hand, for indoor environments, the FFT modules would generate too much latency, therefore it is more judicious to use FIR filters.

In order to have a suitable trade-off between complexity and latency, two solutions are necessary: a time domain approach with FIR filters for the indoor environment and a frequency domain approach with FFT modules for the outdoor environment.

The FIR filter carries out convolutions. Several multipliers are used, their number depends on the length of the channel impulse response. The frequency domain approach uses only one multiplication but needs, for each SISO channel, one FFT module and one IFT module, which increases the latency of the digital block.

Fig. 7 describes the architecture of the digital block for both frequency domain and time domain.

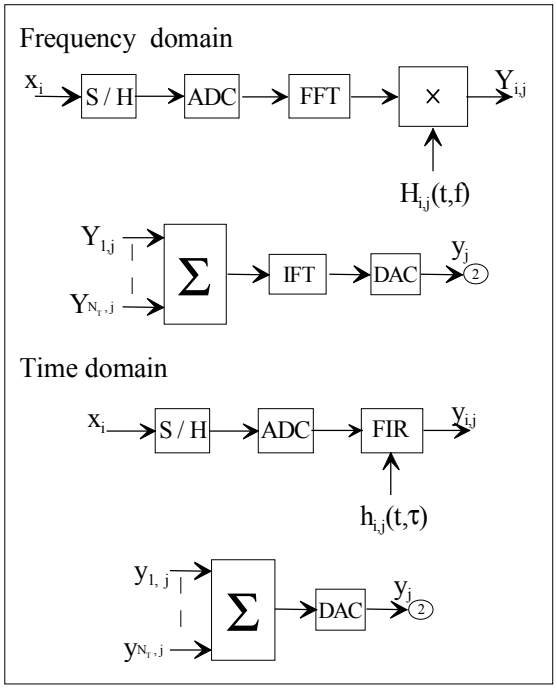

Fig. 7. Digital block.

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For an outdoor environment, the digital block operates in the frequency domain. The Fourier transform of the input signal, obtained at the output of the FFT block, is multiplied by the channel frequency response $H_{i,j}(t,f)$, which includes the correction of errors introduced by the filters of the reception unit. Then, the sum must be realized N_R times, to add each SISO $Y_{i,j}(t,f)$ signal coming from each simulator input. This signal is truncated depending on the number of data bits of the D/A converter. Finally, from the resulting MIMO signal $Y_j(t,f)$ representing the sum of the SISO $Y_{i,j}(t,f)$ signals, the IFT block gives the low-frequency output signal $y_j(t,\tau)$ which represents the input of the transmission RF unit.

For an indoor environment, the digital block operates in the time domain. The FIR filter block computes the convolution product between the sampled input signal and the channel impulse response $h_{i,j}(t,\tau)$. As for the frequency domain, the sum must be realized N_R times to add the SISO $y_{i,j}(t,\tau)$ signals coming from each simulator input. Then, each sum must be truncated according to the number of data bits of the D/A converter.

By using the Shannon theorem and the expected performances of the RF/IF filters, the sampling frequency f_s is 40 MHz for UMTS systems and 50 MHz for WLAN systems. This choice allows a reasonable low sampling rate and avoids the aliasing problems.

According to the considered propagation environments, Table 1 summarizes some useful parameters.

Table 1. Simulator parameters.

	Type	Cell Size	$W_{t\,eff}(\mu s)$	N	$W_t(\mu s)$
UMTS	Rural	2-20 km	20	512	12.8
(B = 15 MHz)	Urban	0.4-2 km	3.7	128	3.2
(fs = 40 MHz)	Indoor	20-400 m	0.7	28	0.7
WLAN	Office	40 m	0.39	20	0.4
(B = 20 MHz)	Indoor	50-150 m	0.73	37	0.74
(fs = 50 MHz)	Outdoor	50-150 m	1.16	64	1.28

For these various environments, the size of the FFT blocks is estimated by:

$$N = \frac{W_t}{T_s} = W_t f_s \qquad (3)$$

where W_t represents the width of the effective time window of the impulse response of the propagation channel, i.e. the width of the time-interval where the impulse response can be considered not null. The final value N is the closest 2^n value (for FFT only). The resulting W_t is also given in Table 1.

If the latency of the "Digital block" is lower than the absolute delay of the first path τ_0 , no error will occur.

III. Implementation

In order to implement the hardware simulator, several solutions of prototyping platforms were studied. The adopted solution uses a prototyping platform based on 3 development boards (XtremeDSP Development Kit-IV for Virtex-4) from Xilinx [6], shown in Fig. 8.

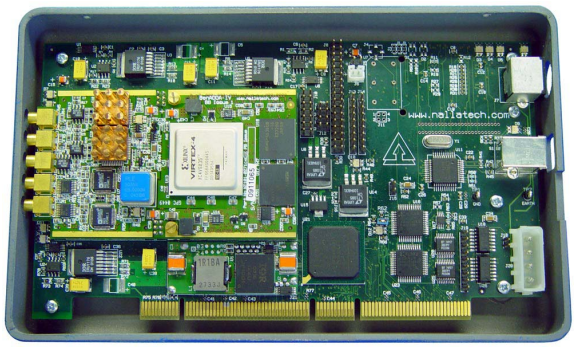

Fig. 8. XtremeDSP Development Kit-IV for Virtex-4.

A. Description

The XtremeDSP Development Kit provides a complete platform for high-performance signal processing applications. This kit features dual-channel high-performance ADCs (AD6645) and DACs (AD9772A) with 14-bit resolution, a user programmable Virtex-4 FPGA, support for external clock, programmable clocks, two banks of ZBT-SRAM, host interfacing via PCI or USB, and JTAG interfaces.

This development kit is built with a module containing the Virtex-4 SX35 component selected to correspond to the complexity constraints. It contains a number of arithmetic blocks (DSP blocks) which makes it possible to implement many functions occupying most of the component.

In addition, the digital block must operate with relatively high frequencies, in order to share the limited resources on several clock cycles.

This device enables us to implement not only the FIR filter for the time domain but also the FFT module for the frequency domain and thus to reprogram the component according to the selected (indoor or outdoor) environment.

B. Implementation and results

According to Table 1, the worst case for indoor environments uses a FIR filter with a length of 64. So, for the time domain, we have developed our own FIR filter with a length of 64, instead of using Xilinx MAC FIR filter because this filter does not make it possible to reload the FIR filter coefficients. According to the resolution of the A/D and D/A converters, our own filter has a 14 bits resolution for input and output data. It has also a 16 bits resolution for the coefficients of the impulse response of the channel. The coefficients have a power of two resolution to optimize the memory size. In addition, each intermediate product of the FIR is truncated on 20 bits.

Before each FIR operation, the 64 coefficients of each FIR are stored first in 14 shift registers of length 64 via USB ports of each board. Then, they are stored in the FPGA dual-port RAM. So, it is possible to prepare the loading of the next coefficients in the register. Those coefficients are read at 100 MHz and the input data at 50 MHz. Thus, the same FIR multipliers are used during two cycles. A binary arborescent structure of adders makes it possible to build a 4-stages pipeline.

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Several simulations and synthesis was made with Xilinx ISE and Modelsim software. Table 2 shows the device utilization for 4 FIR 64 in one V4-SX35 after synthesis, mapping and place & route. For example, 128 DSPs are used and DSPs occupy 66 % of available DSPs.

Table 2. Virtex-4 SX35 utilization for 4 FIR 64:

Number of Slices	10015 out of 15360	65%
Number of logic LUTs	7586 out of 30,720	24%
Number of RAM LUTs	4096 out of 30,720	14%
Number of Flip Flops	9,680 out of 30,720	31%
Number of DSP48s	128 out of 192	66%
Clock period	9,92 ns	

For the frequency domain, the Fourier transform is realized with the FFT module from Xilinx. As the development kit has 2 ADC and 2 DAC, it can be connected to only 2 antennas, so we have to use 2 FFT and 2 IFT per FPGA. The V4-SX35 utilization summary is given in the Table 3 for one FFT with a length of 512, which is the worst case for outdoor environments according to Table 1.

Table 3. Virtex-4 SX35 utilization for 1 FFT 512:

Number of Slices	2,638 out of 15,360	17%
Number of logic LUTs	2,716 out of 30,720	8%
Number of RAM LUTs	1,132 out of 30,720	3%
Number of Flip Flops	3,253 out of 30,720	10%
Number of DSP48s	16 out of 192	8%
Clock period	6,8 ns	

To determine the digital block latency, the used FIR filter and FFT block latency are measured.

The FIR filter block has 4 stages, so 4 clock cycles (2 cycles of 32 multiplications and 2 addition cycles). Then, an addition cycle is necessary to add the results of each FIR. Thus, we have 5 cycles at 100 MHz, therefore 50 ns of latency for the FIR. It is necessary to add approximately 38 ns of the ADC latency, and 17 ns of the DAC latency, according to their respective datasheet.

The FFT block latency is measured between the time when the data enter in the FFT block and the time when the result is provided, which is roughly a latency of 5 µs.

Moreover, for a MIMO configuration, we have to use several boards connected together with point-to-point links. Thus, synchronization differences between boards also add a latency of several ns. So, it is necessary to add one clock cycle for communication between boards for both frequency and time domains.

In summary, the digital block and the converters have a latency of 5 µs for the frequency domain and 115 ns for the time domain.

IV. Conclusion

SIMPAA2 project has two main objectives. The first objective concerns the design and the realization of the digital block of the hardware simulator by using a prototyping platform containing programmable circuits. The second objective concerns the reliable MIMO channel models which must supply the digital block.

After a comparative study, in order to reduce the complexity and the latency of the digital block, the output signal of the MIMO simulator will be computed in the frequency domain for outdoor environments and in time domain for indoor environments.

This work will be continued to complete the design of the architecture of the hardware simulator by minimization of the latency of the digital block and maximization of its precision.

Nowadays, we work with a configuration which requires 3 XtremeDSP Development Kit-IV but we are studying a 200 MHz optimized FIR filter solution allowing to reduce the latency from 115 ns to 90 ns. Synchronization effects on latency will be precisely measured with these three boards.

More measurement campaigns will be carried out with the MIMO channel sounder, realized by IETR, for various types of environments (indoor, outdoor, penetration) and for both UMTS and WLAN frequency bands. The final objective of these measurements is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator.

Lastly, the digital block of the MIMO hardware simulator will be implemented as an electronic module. A Graphical User Interface (GUI) will be also developed to allow the user to configure the channel parameters: environment type, channel model, time window, mobile speed, etc.

Acknowledgments

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